Amendments to the Specification:

Please amend the paragraph beginning on page 6 at line 16 as follows:

A differential data input is provided to the half-rate phase detector 210 on data lines 135. Alternately the data input may be single ended. Demuliplexed data is provided on lines 215 and 217. The half-rate phase detector compares data on lines 135 with the clock signals on line [[145]] 147, and outputs an ERROR signal on line 222 that is proportional to the phase error between the clock and data signals. The half-rate phase detector 2 1 0 provides this ERROR signal on line 222, as well as a REFERENCE signal on line 224 to charge pump 220. The REFERENCE signal on line 224 is a data dependent signal which is used to correct for the data dependence of the ERROR signal on line 222. Charge pump 220 provides a correction signal that is filtered by low-pass filter 230, and sent to the VCO 240. VCO 240 provides the differential clock signal on line 147 which is used by the half-rate phase detector 210 for retiming the data input signal. These blocks form a feedback loop in which a clock signal is extracted from an incoming data stream, and used to retime the data.

Please amend the paragraph beginning on page 10 at line 11 as follows:

To improve performance, [[sone]] some circuit delay time and trace paths should be matched to each other. Specifically, the first latch clock-to-output delay and the traces coupling the first latch to the second latch and the XOR gate 540 should match the third latch clock-to-output delay and the traces coupling the third latch to the fourth latch and the XOR gate 540. Also, the second latch clock-to-output delay and the traces coupling the second latch to the buffer 530 and the XOR gate 550 should match the fourth latch clock-to-output delay and the traces coupling the fourth latch to the buffer 580 and the XOR gate 550.

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Please amend the paragraph beginning on page 12 at line 5 as follows:

An alternate embodiment for an XOR gate can be found in commonly assigned U.S. provisional patent application Ser. number [[_____]] 60/183,169, filed [[_____]] February 17, 2000, titled "Linear Full-Rate Phase Detector and Clock [[and]] Data Recovery Circuit Using the Same," attorney docket number 019717-001210US~~, which is incorporated by reference~~. Also, other architectures which may be used to implement some of the circuits herein can be found in commonly assigned U.S. ~~patent application Ser. No. _____, filed _____,~~ Patent No. 6,424,194, filed January 18, 2000, titled "[[C^3MOS]] Current Controlled CMOS

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Logic Family," attorney docket number 019717-000310US, which is incorporated herein by reference.

Please amend the paragraph beginning on page 14 at line 14 as follows:

If the data is not random, for instance if DATA 910 is a long string of either high or low data bits, then ERROR pulses, such as 906, and REFERENCE pulses, such as 917 are low. The [[of the]] ERROR signal's average value is at a minimum, as is the REFERENCE signal 970. But if the data changes every bit, then each ERROR signal pulse and each REFERENCE bit is high. Therefore the ERROR signal is equal to half its peak value and the REFERENCE signal equals its peak value. Thus, the ERROR signal and REFERENCE signal divided by two have the same data pattern dependency, while the ERROR signal also tracks the phase error. This means the data dependency of ERROR signal 940 can be corrected by subtracting half the average value the REFERENCE signal 970. From a circuitry implementation, this means in FIG. 7, PMOS mirror devices M7 750 and M8 755 should be scaled differently for XOR gates 540 and 550 in FIG. 5. Specifically, either M8 can be doubled, or M7 can be halved in XOR gate 540 as compared to XOR gate 550. The difference signal between the ERROR and one-half the REFERENCE signals is not dependent on the data pattern, but is dependent on the phase error. This resulting signal has approximately a zero value when the DATA signal's edges are aligned with the center between the CLOCK

edges. As the DATA is delayed, the differential value becomes negative. As the DATA advances, the difference becomes positive.